A Technique for Modelling *S*-Parameters for HEMT Structures as a Function of Gate Bias

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***Abstract*—A physically based technique for modelling HEMT structure *S*-parameters is presented. The core of the model is directly dependent on the HEMT wafer structure and the physical gate length. The model accurately predicts the device's *S*-parameters as a function of the applied gate bias. The physical basis facilitates the modelling of different types of HEMT structures. In this paper we present measured *S*-parameters and simulation results, over a frequency range of 1 to 25 GHz, for three different HEMT structures: uniformly-doped, GaAs-channel; pulse-doped, GaAs-channel; and uniformly-doped, strained-InGaAs-channel.**

I. Introduction

PRESENT equivalent-circuit *S*-parameter models for HEMTs consist of a network of resistors, capacitors, inductors and a voltage controlled time-dependent conductance. Such an equivalent circuit is illustrated in Fig. 1. In this figure C1, C2 and C3 are pad-to-pad capacitances and *Rg*, *Lg*, *Rs*, *Rd* and *Ld* are the resistance and inductance associated with the gate, source and drain respectively. *Cds* is the drain-source capacitance, *Cgd* is the gate-drain capacitance and *Ri* represents the resistive path for the charging of the gate-source capacitance, *Cgs*. The output conductance is *gds* and the transconductance, *gm*, includes a time constant, τ (not shown in the figure), to model the transit time of electrons from source to drain.

This circuit topology reflects the basic physical operation of the device but typically all the element values are determined from measurements by optimisation of the *S*-parameter fit; none are determined from an understanding of the device physics. The lack of a physical basis for the element values inhibits the equivalent circuit from efficiently modelling the *S*-parameter bias dependence which is necessary for designing circuits such as digital circuits and power amplifiers. Non-physical models, such as [1], can predict *S*-parameter bias dependence but require a very large number of fitting coefficients. Physical models are useful since they enable efficient modelling of the *S*-parameter bias dependence and provide a link between technological parameters and electrical performance.

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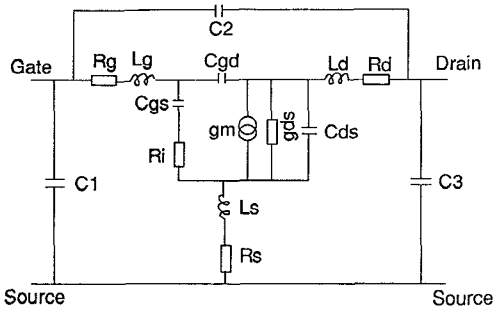

Fig. 1. HEMT equivalent circuit. C1, C2 and C3 are pad-to-pad capacitances.

Yeager and Dutton [2] reported a SPICE-compatible model that calculated the *Y*-parameters of a uniformly-doped, GaAs-channel HEMT with modest agreement to the measured data over a range of biasses at 4 GHz. Roblin *et al.* [3], [4] reported models that calculated the *Y*-parameters, and *S*-parameters, of a uniformly-doped, GaAs-channel HEMT at a fixed gate bias, with an improved fit over a frequency range of 2 to 18.4 GHz. The results presented in these three models rely on parameters fitted to the dc *I–V* characteristics of the HEMT rather than to the physical description of its wafer structure. Eskandarian [5] determined the bias dependence of the gate-source and gate-drain capacitance, transconductance and output conductance by first order perturbation of the Roblin and Rohdin dc HEMT model [6]. Eskandarian reported reasonable agreement between the shape of the calculated transconductance curve and dc measurements at high gate voltages. However, near pinch-off the agreement was poor and no measured results were presented for the output conductance or the capacitances. All these models ignore the influence of the parallel conduction path in the AlGaAs layers (i.e., the so-called "parasitic MESFET") which has been shown to be important for accurate HEMT modelling [7].

This paper presents a physically based model that describes the core HEMT equivalent circuit elements, i.e., the transconductance, output conductance, gate-source capacitance and gate-drain capacitance, as functions of the applied bias. The model, which includes the influence of the parasitic MESFET, is a function of the HEMT wafer structure and physical gate length.

The core HEMT model consists of two parts. The first uses a Poisson/Fermi–Dirac solver to model the electron

density in the current conduction paths from a description of the wafer structure. The second uses analytical expressions to determine the transconductance, output conductance, gate-source capacitance and gate-drain capacitance from the physical gate length, the output of the Poisson/Fermi–Dirac solver and some empirical constants. The device model is completed by incorporating the empirically determined C1, C2, C3, *Rg*, *Rs*, *Rd*, *Lg*, *Ls*, *Ld*, *Cds* and *Ri*, which are assumed to be bias independent. The resultant model successfully predicts the *S*-parameters for a variety of different HEMT structures (uniformly-doped, GaAs-channel; pulse-doped, GaAs-channel; and uniformly-doped, strained-InGaAs-channel) over a wide range of biasses and frequencies (1 to 25 GHz).

In Section II the *S*-parameter model is described. Section III presents a comparison of model results with *S*-parameter measurements on three different HEMT structures. For each structure, model results are presented for a "best-estimate" set of parameters, i.e., a set of parameters that could reasonably be estimated for a well-controlled fabrication process. Best-estimates for the wafer structure and gate length are obtained by destructive measurement of similar devices. Best-estimates for electron velocities are guided by results reported in the literature. Also for the uniformly-doped, GaAs-channel device the inverse modelling technique described in [8], [9], extended to operate on *S*-parameters, is used to fine tune the values of the parameters describing the wafer structure. This improves the fit between modelled and measured *S*-parameters. Concluding remarks are presented in Section IV.

II. Scattering Parameter Model

The three different HEMT structures studied in this paper are illustrated in Fig. 2. In describing these structures, the vertical dimension measured from the heterojunction towards the gate is z.

The Poisson/Fermi–Dirac solver is described in Section II-A. The core analytical model, which is derived from the output of the Poisson/Fermi–Dirac solver, is described in Section II-B. The calculation of the *S*-parameters for the devices from the bias independent components and the core analytical model is described in Section II-C.

A. Poisson/Fermi–Dirac Solver

The electron density in the two dimensional electron gas (2DEG) and in the layers between the heterojunction ($z = 0$) and the gate are determined numerically by solving Poisson's equation using Fermi–Dirac statistics for the electrons. The Poisson/Fermi–Dirac solver starts by assuming a value for the 2DEG density. For a GaAs-channel, Delagebeaudeuf and Linh's triangular well approximation (with empirically determined coefficients used to fit the dependence of the energy levels upon the electric field) [10] is solved exactly to give the depth of the heterojunction notch below the Fermi level. A 60% rule [11]

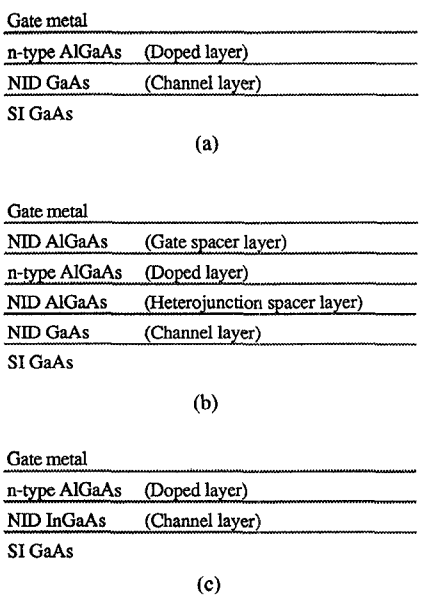

Fig. 2. Description of the three HEMT wafer types modelled in this paper. (a) Uniformly-doped with GaAs channel, (b) pulse-doped with GaAs channel, (c) uniformly-doped with strained-InGaAs channel. NID = Not Intentionally Doped, SI = Semi-Insulating.

is then used to calculate the conduction band edge immediately on the gate side of the heterojunction ($Ec(z = 0^+)$). In the case of an InGaAs-channel, strained between AlGaAs and GaAs, the sequence of bound states is calculated within the triangular well approximation with an additional boundary-value matching of wave-function solutions at the InGaAs/GaAs interface. The solutions are given by appropriate linear combinations of Airy functions. The strain-induced renormalisation of the effective InGaAs bandgap is calculated according to Pötz and Ferry [12].

The slope of the conduction band edge at the heterojunction is calculated from the assumed 2DEG density, n_s, using Gauss' law

$$\left.\frac{dEc(z)}{dz}\right|_{z=0^+} = \frac{-q \cdot n_s}{\epsilon} \tag{1}$$

where ϵ is the permittivity and q is the electronic charge. From the boundary conditions $Ec(z = 0^+)$ and $dEc(z)/dz|_{z=0^+}$, the technique described by Ponse *et al.* [13] is used to determine the Fermi level and the conduction band edge between the heterojunction and the gate. The accuracy of Ponse's technique is improved by using Bednarczyk's formula [14] to approximate the Fermi–Dirac integral, Chand's results [15] for the donor activation energy as a function of the aluminium fraction and Casey and Panish's formula [16] for the density of conduction band states as a function of the aluminium fraction. The gate voltage is the negative of the Fermi level at the gate provided that the gap between the conduction band edge and the Fermi level at the gate is within some acceptable tolerance (typically 0.1 mV) of the 0.8 V built-in voltage. If this condition is not met then the gate current is adjusted and the Ponse technique repeated. Oth-

erwise the assumed value of the 2DEG density is incremented and the whole process repeated. The two dimensional electron density in the layers between the gate and the heterojunction is easily obtained by trapezoidal integration of the conduction band electron density at each distance step of Ponse's process.

B. Core Analytic Model

In our dc HEMT model [8], [9] the number density of the 2DEG as a function of the gate-channel voltage, $n_s(Vgc)$, is modelled by

$$n_s(V - Vgc = Vto) = \begin{cases} 0 & V \le 0 \\ \dfrac{c \cdot V^2}{1 + a \cdot V^2 + b \cdot V^3} & \text{otherwise} \\ n_{so} & V > \sqrt[3]{\dfrac{2}{b}} \end{cases} \quad (2)$$

where a, b, c and Vto are parameters to be determined by fitting this equation to the 2DEG electron density obtained from the Poisson/Fermi–Dirac solver. An accurate model also requires modelling of the current carrying electrons in the parasitic MESFET that forms in the layers between the heterojunction and the gate. The MESFET electron density, $n_a(Vgc)$, is given by

$$n_a(V = Vgc - mVto) = \begin{cases} 0 & V \le 0 \\ ma \cdot V^2 + mb \cdot V^3 & \text{otherwise} \end{cases} \quad (3)$$

where ma, mb and $mVto$ are parameters determined by fitting this equation to the conduction band electron density in the layers between the heterojunction and the gate, as obtained from the Poisson/Fermi–Dirac solver. By accurately fitting (2) and (3) to the electron densities calculated by the Poisson/Fermi–Dirac solver, information about the wafer structure (i.e., the layer thicknesses, doping densities, aluminium and, if appropriate, indium fractions) is embedded in the values of the parameters a, b, c, Vto, ma, mb, and $mVto$. Typically (2) and (3) can be fitted to the numerical electron density data with a relative rms error of around 1%.

Calculation of Transconductance and Output Conductance: From (2) the current carried by the 2DEG, Ids_{2DEG}, is calculated by

$$Ids_{2DEG}(Vgs, Vds) = \begin{cases} 0 & Vds < 0 \\ \left(1 - \left(1 - \dfrac{Vds}{Vdss}\right)^2\right) \cdot Idss_{2DEG} & \text{otherwise} \\ Idss_{2DEG} & Vds > Vdss \end{cases} \quad (4)$$

where $Idss_{2DEG} = q \cdot W \cdot n_s(Vgs' - Vdss) \cdot v_{sat} \cdot (1 + \lambda \cdot Vds)$, W is the device width, $Vgs' = Vgs + \eta \cdot Vds$, Vgs is the gate-source voltage (i.e. Vgc at the source end of the channel), Vds is the drain-source voltage, η is a parameter describing drain feedback [17]–[19], v_{sat} is the electron velocity, λ is a parameter describing channel length modulation [20]–[22] and the drain-source saturation voltage (or "knee-voltage"), $Vdss$, is a function of Vgs', a, b, c, Vto and the electrical gate length, L_e [8], [9].

The parasitic MESFET current is calculated using a formula similar to that used for the 2DEG current. Hence, for the parasitic MESFET

$$Ids_{MES}(Vgs, Vds) = \begin{cases} 0 & Vds < 0 \\ \left(1 - \left(1 - \dfrac{Vds}{mVdss}\right)^2\right) \cdot Idss_{MES} & \text{otherwise} \\ Idss_{MES} & Vds > mVdss \end{cases} \quad (5)$$

where $Idss_{MES} = q \cdot W \cdot n_a(mVgs' - mVdss) \cdot mv_{sat} \cdot (1 + m\lambda \cdot Vds)$, $mVgs' = Vgs + m\eta$. Vds, $m\eta$ is a parameter describing drain feedback, mv_{sat} is the electron velocity, $m\lambda$ is a parameter describing channel length modulation and $mVdss$ is a function of $mVgs'$, ma, mb, $mVto$ and L_e [8].

Wasserstrom and McKenna [23] linked the physical gate length, L_p, to the effective (electrical) gate length, L_e, based on numerical analysis of a metal strip on the surface of a homogenous semiconductor. Their work has been adapted to the HEMT case by assuming that the HEMT wafer is equivalent to a homogenous semiconductor with relative permittivity equal to that of the wide bandgap material. Hence for $Al_xGa_{1-x}As/GaAs$ and $Al_xGa_{1-x}As/In_yGa_{1-y}As/GaAs$ devices

$$L_p = L_e - d_a \cdot \left(1.416 + \frac{1.82}{13.1 - 3 \cdot x}\right) \quad (6)$$

where d_a is the total thickness of the $Al_xGa_{1-x}As$ layers.

The total drain-source current, Ids, is the sum of Ids_{2DEG} and Ids_{MES}. The device transconductance, gm, is the differential of Ids with respect to Vgs, multiplied by a delay term to model the electron transit time from source to drain,

$$gm(Vgs, Vds) = \left(\frac{dIds_{2DEG}}{dVgs} + \frac{dIds_{MES}}{dVgs}\right) \cdot e^{-j \cdot 2 \cdot \pi \cdot f \cdot \tau} \quad (7)$$

where $j = \sqrt{-1}$, f is the frequency and τ is the transit time constant. The device output conductance, gds, is the differential of Ids with respect to Vds,

$$gds(Vgs, Vds) = \frac{dIds_{2DEG}}{dVds} + \frac{dIds_{MES}}{dVds} \quad (8)$$

The accuracy of the conductances calculated by (7) and (8) may be degraded for large signal modelling applications by the relatively long capture and release time of *dx*-center traps in devices with aluminium fractions greater than 25%. Such problems are minimized, as done with the devices examined here, by avoiding high aluminium fractions.

Calculation of Gate-Source and Gate-Drain Capacitance: In the linear region the charge under the gate, Q, is assumed to be linearly distributed along the channel,

$$Q(Vgs, Vgd = Vgs - Vds) = \frac{q \cdot W \cdot L_e \cdot (n_s(Vgs) + n_s(Vgd) + n_a(Vgs) + n_a(Vgd))}{2} \quad (9)$$

When either conduction path enters the saturated region ($Vds > (m)Vdss$) the electron density at the drain end of the channel becomes only a weak function of Vgd. In [24] this weak dependence was modelled by replacing $n_s(Vgd)$ with $n_s(Vgd')$ and $n_a(Vgd)$ with $n_a(\mathrm{mV}gd')$ in (8), where

$$Vgd'(Vgs) = \begin{cases} Vgd & Vds < \left(2 - \frac{1}{\gamma}\right) \cdot Vdss \\ Vgs - \left(1 - \beta \cdot \left(1 - \frac{\gamma \cdot Vds}{Vdss}\right)^2\right) & \\ \cdot Vdss & \text{otherwise} \\ Vgs - Vdss & Vds > \frac{Vdss}{\gamma} \end{cases} \quad (10a)$$

where $\beta = [1/4 \cdot \gamma \cdot (1 - \gamma)]$ and

$$mVgd'(Vgs) = \begin{cases} Vgd & Vds < \left(2 - \frac{1}{m\gamma}\right) \cdot mVdss \\ Vgs - \left(1 - m\beta \cdot \left(1 - \frac{m\gamma \cdot Vds}{mVdss}\right)^2\right) & \\ \cdot mVdss & \text{otherwise} \\ Vgs - mVdss & Vds > \frac{mVdss}{m\gamma} \end{cases} \quad (10b)$$

where $m\beta = [1/4 \cdot m\gamma \cdot (1 - m\gamma)]$. The variables γ and $m\gamma$ are transition smoothing parameters. Both γ and $m\gamma$ must not be less than 0.5 to ensure continuity at $Vds = 0$ V and they must be less than 1.0 for the smoothing transition region to exist. Typically, γ and $m\gamma$ are set to a compromise value of 0.75.

The gate-source capacitance, $Cgs(Vgs, Vds)$, is the partial derivative of Q with respect to Vgs, plus a term $Cgsp \cdot (1 + ngs \cdot Vgs)$,

$$Cgs(Vgs, Vds) = \frac{q \cdot W \cdot L_e}{2} \cdot \left(\left(1 + \frac{dVgd'}{dVgs}\right) \cdot \frac{dn_s}{dVgs} + \left(1 + \frac{dmVgd'}{dVgs}\right) \cdot \frac{dn_a}{dVgs}\right) + W \cdot (Cgsp(1 + ngs \cdot Vgs)) \quad (11)$$

The gate-drain capacitance, $Cgd(Vgs, Vds)$, is the partial derivative of Q with respect to Vgd, plus a term $Cgdp \cdot (1 + ngd \cdot Vgd)$,

$$Cgd(Vgs, Vds) = \frac{q \cdot W \cdot L_e}{2} \cdot \left(\frac{dVgd'}{dVgd} \cdot \frac{dn_s}{dVgd} + \frac{dmVgd'}{dVgd} \cdot \frac{dn_a}{dVgd}\right) + W \cdot (Cgdp(1 + ngd \cdot Vgd)) \quad (12)$$

In (11) and (12) the terms $Cgsp \cdot (1 + ngs \cdot Vgs)$ and $Cgdp \cdot (1 + ngd \cdot Vgd)$ model, on a phenomenological basis, two identifiable physical effects. The first is modulation of the depletion region in the semiconductor below the gap between the gate and the n^+ GaAs capping layer. The capacitance associated with this depletion region increases as it shrinks in response to increased gate voltage. This is modelled by a positive value of *ngs* and *ngd*. The second effect is the control, by the gate's electric field, of the small capacitance due to holes in the substrate layer. Ando and Itoh [25] showed that this effect decreases with increasing gate voltage and hence is modelled in (11) and (12) by a negative value of *ngs* and *ngd*, respectively. In the simulations presented here *ngs* and *ngd* can take either sign depending on the relative influence of these two effects.

The core HEMT model for the device drain current (*Ids*), given by the sum of (4) and (5), the transconductance, given by (7) without the exponential term, the output conductance, (8), the charge, (9) and the gate-source and gate-drain capacitance, (11) and (12) respectively, have also been implemented in SPICE 3 and used successfully to simulate logic circuits [26].

C. Calculation of Scattering Parameters

The transconductance, output conductance, gate-source capacitance and gate-drain capacitance, along with the bias independent components of the HEMT equivalent circuit in Fig. 1, are used to calculate the impedance matrix for the device using Kirchhoff's laws. The scattering parameters are then calculated from the elements of the impedance matrix using the transformation in [27].

The entire modelling process, from the beginning of the Poisson/Fermi–Dirac solver through to the calculation of the four scattering parameters, for six bias points and 25 different frequencies takes less than a minute on a Sun SPARC 1 workstation.

III. Results and Discussion

The uniformly-doped GaAs-channel device, pulse-doped GaAs-channel device, and uniformly-doped strained-InGaAs-channel device were modelled using the techniques described in Section II.

TABLE I
PERCENTAGE ERROR BETWEEN THE MEASURED *S*-PARAMETERS AND THOSE PREDICTED BY THE MODEL USING i) BEST-ESTIMATE PARAMETERS AND ii) FINE-TUNED PARAMETERS FOR THE UNIFORMLY-DOPED, GaAs-CHANNEL DEVICE (SH94-5G)

Scattering Parameter	Percentage Error (Best-Estimate)	Percentage Error (With Fine-Tuning)
s_{11}	2.37	2.31
s_{12}	2.18	2.10
s_{21}	2.10	1.92
s_{22}	5.34	4.99
Average	3.00	2.83

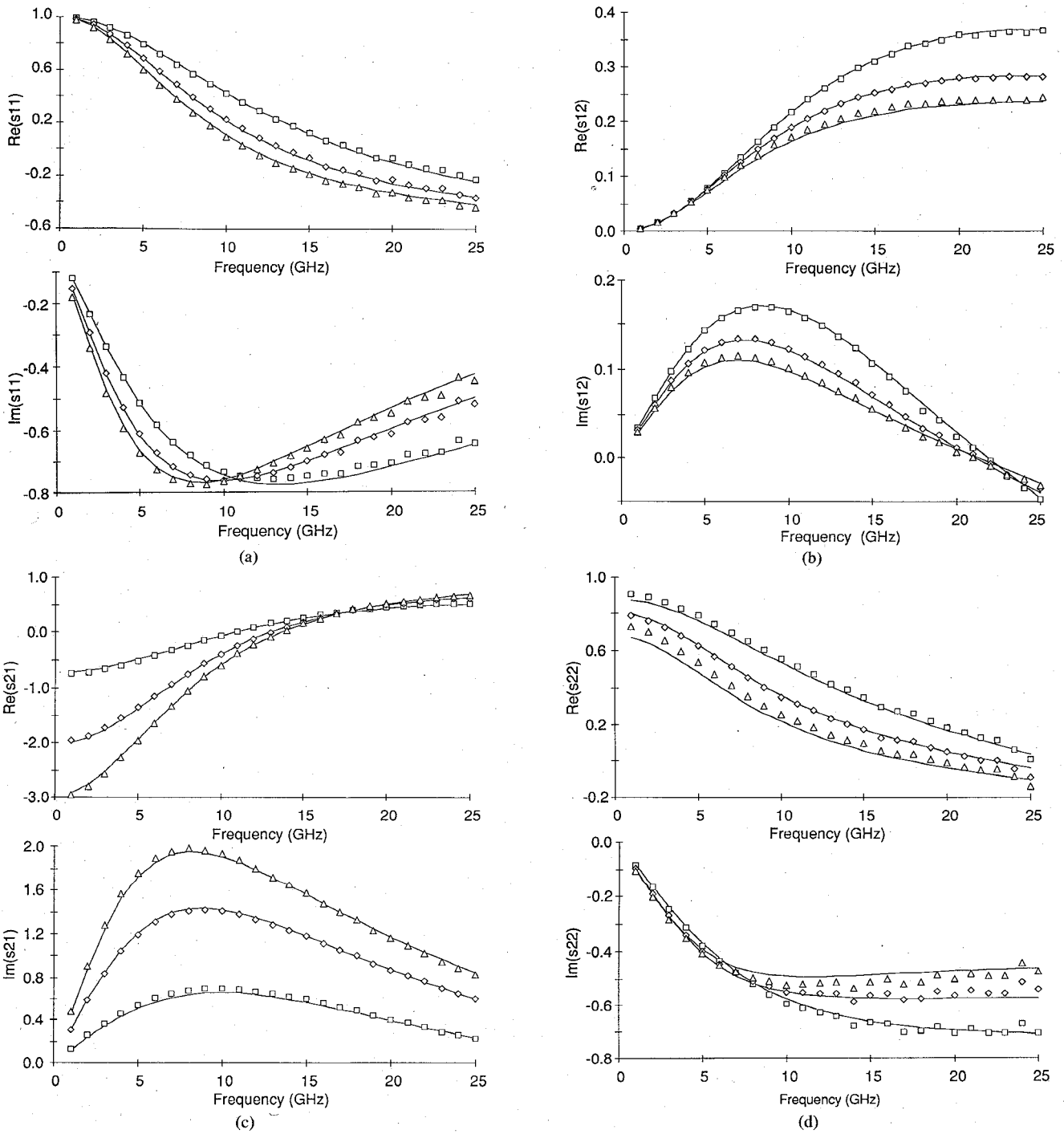

Fig. 3. The real and imaginary parts of (a) s_{11}, (b) s_{12}, (c) s_{21} and (d) s_{22} for a uniformly-doped, GaAs-channel device (SH94-5G). The biasses are $Vgs = -0.25$ V (□), -0.10 V (◇) and 0.00 V (△) ($Ids = 0.4$ to 6.0 mA at $Vds = 2.0$ V) and the frequency range is 1 to 25 GHz.

TABLE II
THE VALUE OF THE PARASITIC PARAMETERS USED FOR THE UNIFORMLY-DOPED, GaAs-CHANNEL DEVICE (SH94-5G)

	Value	Units		Value	Units		Value	Units
Rg	8.56	Ω	*Rs*	0.30	Ω · mm	*Rd*	0.30	Ω · mm
Lg	57.8	pH	*Ls*	≈0	pH	*Ld*	19.2	pH
C1	35.3	fF	C2	27.3	fF	C3	1.82	fF
Ri	≈0	Ω	τ	2.08	ps	*Cds*	35.8	fF
λ	≈0	V^{-1}	$m\lambda$	0.84	V^{-1}	η	0.65	—
$m\eta$	0.061	—	*ngs*	≈0	V^{-1}	*ngd*	1.54	V^{-1}
Cgsp	18.6	$pF \cdot m^{-1}$	*Cgdp*	52.6	$pF \cdot m^{-1}$			

Measurements were taken using a HP8510 Network Analyser and a Cascade Microtech Probe Station from 1 to 25 GHz, and from a low bias to $Vgs = 0$ or to a gate voltage that produces a significant Ids current. The model parameters that depend on the wafer structure (the layer thicknesses, dopant densities and compositional fractions) are almost entirely responsible for the *S*-parameter bias dependence. The wafer structure was determined from average results of direct destructive measurement of similar devices. The layer thicknesses were determined by calibration of the MBE machine using a Tencor Alphastep 100 Surface Profilometer and by TEM cross sections. Spot Hall measurements were used to determine the dopant densities and photoluminescence measurements were used to determine the compositional fractions. The physical gate length was determined by direct measurement (with a SEM) of similar devices. The electron velocity, v_{sat}, in the 2DEG is discussed in each subsection. The electron velocity in the AlGaAs layer is based on the measurements of bulk AlGaAs made by Banerjee *et al.* [28] and incorporates a correction factor of 1.49 to account for velocity overshoot due to the short gate length [8]. This correction factor was derived from analysis of uniformly-doped AlGaAs/GaAs devices with a similar gate length to the devices considered here. Other parameters, including those describing the device parasitics whose contribution to the *S*-parameters is independent of bias, were determined by fitting the model's predictions, within bounds set by the history of the fabrication line, to the measured *S*-parameter data. The model results are compared with *S*-parameter measurements by defining a relative rms error metric

$$\text{Error} = \frac{\sum |s_{ii(\text{measured})} - s_{ii(\text{model})}|^2}{\sum |s_{ii(\text{measured})}|^2} \qquad (13)$$

where $i = 1, 2$ and the summations are over all frequencies and all bias points.

In Section III-A the model described in Section II is used to predict the *S*-parameters of a uniformly-doped, GaAs-channel device as a function of the applied bias from 1 to 25 GHz. In Section III-B a pulse-doped, GaAs-channel device is modelled and in Section III-C a uniformly-doped, strained-InGaAs-channel device is modelled. The devices were fabricated using three separate mask sets.

TABLE III
PERCENTAGE ERROR BETWEEN THE MEASURED *S*-PARAMETERS AND THOSE PREDICTED BY THE MODEL USING THE BEST-ESTIMATE PARAMETERS FOR THE PULSE-DOPED, GaAs-CHANNEL DEVICE (PSH37-10G)

Scattering Parameter	Percentage Error (Best-Estimate)
s_{11}	1.15
s_{12}	3.24
s_{21}	2.50
s_{22}	2.41
Average	2.33

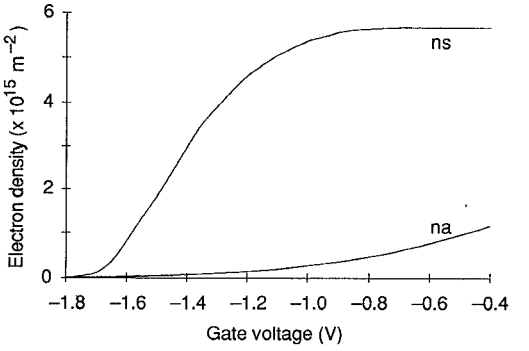

Fig. 4. Calculated electron density in the parasitic MESFET (na) and the 2DEG (ns) as a function of gate voltage for the pulse-doped, GaAs-channel device (PSH37-10G).

For the uniformly-doped, GaAs-channel device the wafer structure is also fine-tuned using the inverse modelling procedure described in [8], [9], extended to operate on *S*-parameters rather than *I–V* characteristics, to improve the fit between the modelled and measured *S*-parameters. Commercial restrictions prohibit publication of the quantitative specification of the wafer structures. Hence, the percentage difference between the measured value and the model value is quoted to facilitate a comparison of the measured parameters with those fine-tuned values used in the model.

A. Uniformly-doped, GaAs-Channel, HEMT

SH94-5G, a 250 μm wide × 0.26 μm long uniformly-doped, GaAs-channel device was measured and modelled from $Vgs = -0.25$ to 0.0 V ($Ids = 0.4$ to 6.0 mA) over the frequency range 1 to 25 GHz. The agreement between the best-estimate model *S*-parameters and the measured *S*-parameters is good for s_{11}, s_{12} and s_{21} and reasonable

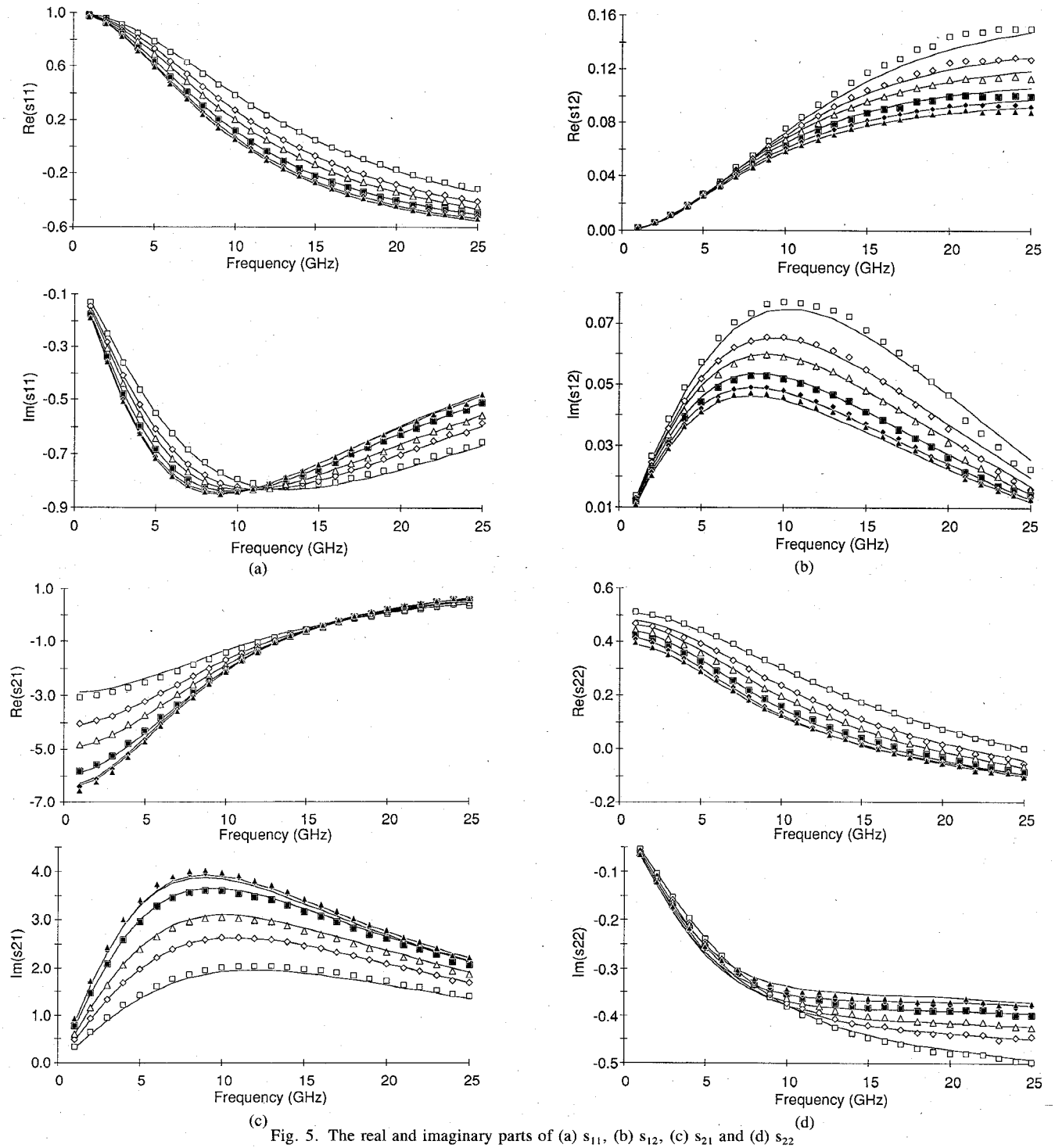

Fig. 5. The real and imaginary parts of (a) s_{11}, (b) s_{12}, (c) s_{21} and (d) s_{22} for a pulse-doped, GaAs-channel devices (PSH37-10G). The biasses are $Vgs = -1.39$ (□), -1.30 V (◇), -1.23 V (△), -1.11 V (■), -0.99 V (♦) and -0.87 (▲) (Ids = 10 to 50 mA at Vds = 2.0 V) and the frequency range is 1 to 25 GHz.

for s_{22} as shown in Table I. The device turn-off voltage is -0.61 V and the measured dc transconductance is 282 S $\cdot$ m^{-1}.

Inverse modelling analysis of uniformly-doped, GaAs-channel devices without a heterojunction spacer layer in [8], [9] suggested that the electron velocity, v_{sat}, in the GaAs-channel is approximately 206 km $\cdot$ s^{-1}. Rohdin [29] and de la Houssaye *et al.* [30] used different techniques to obtain similar estimates for GaAs-channel devices. Hence, vsat was set to 206 km $\cdot$ s^{-1} for this device.

When the inverse modelling procedure [8], [9] is used to fine tune the wafer structure parameters the quality of the fit improves (Table I). The fine tuned value of the doped layer thickness is 0.10% larger, the doping density is 0.42% larger and the aluminium fraction is 0.01% smaller than the measured values. The electron velocities

TABLE IV
THE VALUE OF THE PARASITIC PARAMETERS USED FOR THE PULSE-DOPED, GaAs-CHANNEL DEVICE (PSH37-10G)

	Value	Units		Value	Units		Value	Units
Rg	2.8	Ω	*Rs*	0.33	Ω · mm	*Rd*	0.65	Ω · mm
Lg	30.4	pH	*Ls*	1.6	pH	*Ld*	3.9	pH
C1	16.9	fF	C2	49.1	fF	C3	0.007	fF
Ri	2.8	Ω	τ	2.0	ps	*Cds*	17.3	fF
λ	0.00009	V^{-1}	$m\lambda$	0.025	V^{-1}	η	0.004	—
$m\eta$	0.64	—	*ngs*	0.70	V^{-1}	*ngd*	−1.48	V^{-1}
Cgsp	0.99	$nF \cdot m^{-1}$	*Cgdp*	18.0	$pF \cdot m^{-1}$			

TABLE V
PERCENTAGE ERROR BETWEEN THE MEASURED *S*-PARAMETERS AND THOSE PREDICTED BY THE MODEL USING THE BEST-ESTIMATE PARAMETERS FOR THE UNIFORMLY-DOPED, STRAINED-InGaAs-CHANNEL DEVICE (PH109-12H)

Scattering Parameter	Percentage Error (Best-Estimate)
s_{11}	2.73
s_{12}	3.43
s_{21}	5.65
s_{22}	3.54
Average	3.84

are not altered. Fig. 3 shows the closeness of the agreement between the fine-tuned model and measured *S*-parameters. The data in Fig. 3, and other similar figures that follow, has been presented in Cartesian form rather than on a Smith chart because the latter can inadvertently hide poor fits which involve a frequency shift between measured and model data. Such a shift produces a clear separation of the curves on a Cartesian chart whereas on a Smith chart it merely slides the measured and calculated curves on top of each other. The values of parasitic parameters are typical for the fabrication process and the device layout (Table II). The large drain pad to source pad spacing on the mask set is consistent with the low value of C3. The inductances are small due to the on-wafer probing technique and the value of *Ri* is small due to difficulties in distinguishing its effects from those of τ. The values obtained for *Cgsp* and *Cgdp* for this device, and the others that follow, are typically of the order of tens to hundreds of $pF \cdot m^{-1}$. This is similar to the magnitudes reported by Ando and Itoh [25] and used by Weiler and Ayasli [31].

The agreement between model predictions and measurement taken at positive gate bias is less impressive. The agreement in this region may be improved by the inclusion of voltage dependent conductances in parallel with the gate junction capacitances *Cgs* and *Cgd*. This is the topic of further work.

B. Pulse-Doped HEMT with GaAs-Channel

PSH37-10G, a 250 μm wide × 0.32 μm long pulse-doped, GaAs-channel device was measured and modelled from *Vgs* = −1.39 to −0.87 V (*Ids* = 10 to 50 mA) over the frequency range 1 to 25 GHz. The agreement between the best-estimate model *S*-parameters and the measured *S*-parameters is good for s_{11}, s_{12}, s_{21} and s_{22} as shown in Table III. The device turn-off voltage is −1.74 volts, the measured dc transconductance is 404 $S \cdot m^{-1}$ and f_{max} is 80 GHz. The calculated electron densities in the parasitic MESFET and the 2DEG are shown in Fig. 4.

The fits given in Table III required the electron velocity, vsat, in the GaAs-channel to be 274 $km \cdot s^{-1}$. This is higher than the figure of 206 $km \cdot s^{-1}$ used for the uniformly-doped, GaAs-channel device and is outside the range reported by Rohdin [29], who found a spread in v_{sat} of approximately 50–60 $km \cdot s^{-1}$ by reverse modelling from the microwave *Y*-parameters of over 100 HEMTs. However, the required high velocity is consistent with the peak electron velocity of approximately 275 $km \cdot s^{-1}$ determined by two independent Monte-Carlo analyses [32], [33]. The increased electron velocity required for the pulse-doped device may be due, at least partially, to the significant heterojunction spacer layer which reduces ionised donor scattering of electrons in the two dimensional gas. Nevertheless, this velocity is substantially less than the figure of 345 $km \cdot s^{-1}$ required by Roblin *et al.* [3, 4] for a GaAs-channel device with a gate spacer layer. This matter needs further investigation.

Fig. 5 shows the closeness of the agreement between the best-estimate model and measured *S*-parameters. There is good agreement between the model predictions and the six measured data-sets. Note especially the compression of s_{21} at high bias due to saturation of the 2DEG density. Here the measured and model values are virtually indistinguishable.

The values of parasitic parameters are again typical for the fabrication process and the device layout (Table IV).

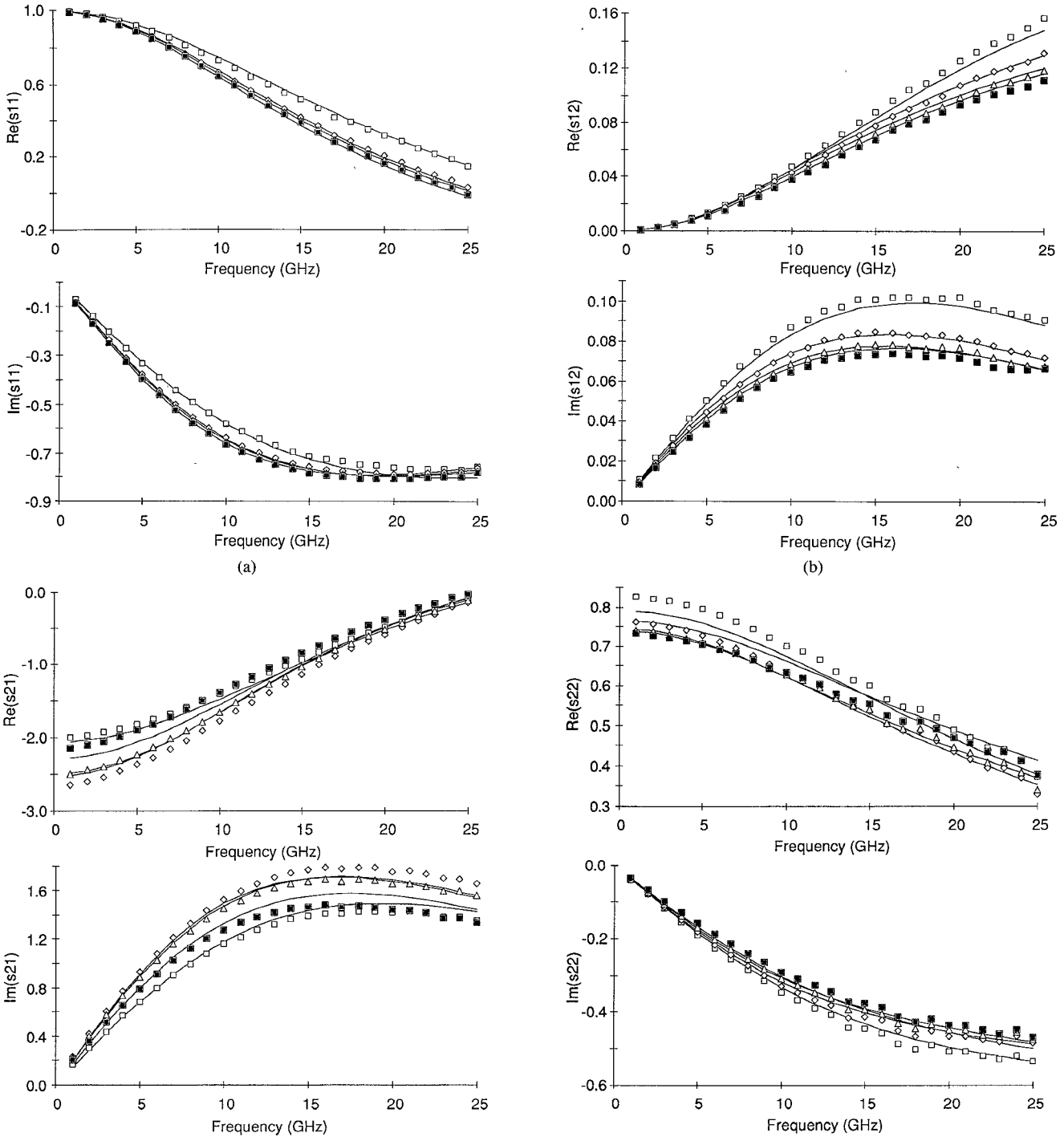

Fig. 6. The real and imaginary part of (a) s_{11}, (b) s_{12}, (c) s_2 and (d) s_{22} for the uniformly-doped, strained-InGaAs-channel device. The biasses are *Vgs* = −1.00 V (□), −0.80 V (◊), −0.60 V (△) and −0.40 V (■) (*Ids* = 3.4 to 25 mA at *Vds* = 2.0 V) and the frequency range is 1 to 25 GHz.

C. Uniformly-doped HEMT with Strained-InGaAs-Channel

PH109-12H, a 125 μm wide × 0.32 μm long uniformly-doped, strained-InGaAs-channel device was measured and modelled from *Vgs* = −1.0 to −0.4 V (*Ids* = 3.4 to 25 mA) over the frequency range 1 to 25 GHz. The agreement between the best-estimate model *S*-parameters and the measured *S*-parameters is good for s_{11}, s_{12} and s_{22} and reasonable for s_{21} as shown in Table V and Fig. 6. The device turn-off voltage is −1.30 V and the measured dc tranconductance is 302 $S \cdot m^{-1}$.

The electron velocity in the InGaAs-channel of a uniformly-doped HEMT is taken to be 172 km/s^{-1} line with

TABLE VI
THE VALUE OF THE PARASITIC PARAMETERS USED FOR THE UNIFORMLY-DOPED, STRAINED-InGaAs-CHANNEL DEVICE (PH109-12H)

	Value	Units		Value	Units		Value	Units
Rg	4.5	Ω	*Rs*	0.58	Ω · mm	*Rd*	0.30	Ω · mm
Lg	0.2	pH	*Ls*	20.2	pH	*Ld*	67.5	pH
C1	27.7	fF	C2	36.0	fF	C3	0.07	fF
Ri	10.3	Ω	τ	1.3	ps	*Cds*	0.04	fF
λ	0.005	V^{-1}	$m\lambda$	1.16	V^{-1}	η	0.10	—
$m\eta$	0.0002	—	*ngs*	−0.34	V^{-1}	*ngd*	−1.29	V^{-1}
Cgsp	2.9	$pF \cdot m^{-1}$	*Cgdp*	29.5	$pF \cdot m^{-1}$			

the results of Dickmann *et al.* [34] and de la Houssaye *et al.* [30]. The latter found InGaAs electron velocities to be approximately 30 km · s^{-1} less than those in GaAs-channels for 0.2 μm gate lengths. The values of parasitic parameters are again typical for the fabrication process and the device layout (Table VI).

IV. CONCLUSION

A technique for modelling HEMT structure *S*-parameters as a function of gate bias and frequency has been presented that is quick, accurate and has a good physical basis. The technique uses a HEMT equivalent circuit model, the core of which uses the device material and geometric parameters, and a set of bias independent parameters, to calculate the gate bias dependence of the transconductance, output conductance, gate-source capacitance and gate-drain capacitance. All other parameters in the HEMT equivalent circuit, including *Ri*, are approximated to be independent of bias.

The model has been successfully demonstrated for three different types of HEMTs; the uniformly-doped AlGaAs with GaAs channel, pulse-doped AlGaAs with GaAs channel and uniformly-doped AlGaAs with strained-InGaAs channel. Using a set of parameters that are the best estimates for the well-controlled fabrication processes, modelled *S*-parameters are within 3.0% (average relative rms) of the measured *S*-parameters for the uniformly-doped, GaAs-channel device, 2.3% of the measured *S*-parameters for the pulse-doped, GaAs-channel device and 3.8% of the measured *S*-parameters for the uniformly-doped, strained-InGaAs-channel device. The results show that accurate modelling of *S*-parameter gate bias dependence (for $Vgs \leq 0$) requires only *gm*, *gds*, *Cgs* and *Cgd* to be bias dependent.

Fine-tuning the parameters that describe the wafer structure using an inverse modelling optimisation improves the agreement between the measured *S*-parameters. For the uniformly-doped, GaAs-channel device this technique reduced the error to 2.8%.

The results presented show that the core model accurately predicts the high frequency *gm*, *gds*, *Cgs* and *Cgd* of the intrinsic device over a range of biasses. Hence, the model is also useful as the basis for the simulation of circuits with large signal waveforms, including digital circuits and power amplifiers, with programs such as SPICE.

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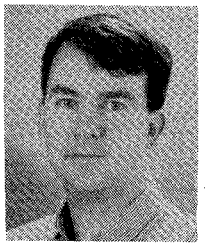

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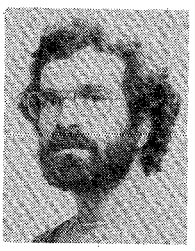

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